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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application No.	10/811,191
Filing Date	March 26, 2004
First Named Inventor	RUECKES, et al.
Art Unit	2818-2823
Examiner Name	TBA Michelle Estrada
Attorney Docket Number	112020.147 US2 NAN-23

Sheet 1 of 1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
[Signature]		US-2005/0041465 A1	02-24-2005	RUECKES, et al.	_____
		US-2005/0041466 A1	02-24-2005	RUECKES, et al.	_____
		US-2005/0056877 A1	03-17-2005	RUECKES, et al.	_____
		US-6,548,841	04-15-2003	FRAZIER et al.	_____
		US-6,803,840	10-12-2004	HUNT et al.	_____
[Signature]		US-6,809,465	10-26-2004	JIN	_____
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		US-			
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FOREIGN PATENT DOCUMENTS

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[Signature]		WO 03/091486 A1	11-06-2003	Nantero, Inc.	[Diagonal line]
		WO 04/065655 A1	08-05-2004	Nantero, Inc.	
		WO 04/065657 A1	08-05-2004	Nantero, Inc.	
		WO 04/065671 A1	08-05-2004	Nantero, Inc.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

Examiner Signature	Michelle Estrada	Date Considered	12/12/05
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		Number-Kind Code ^{2(f) known}			
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		US-4,845,533	07-04-1989	PRYOR ET AL.	
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		US-2003/0165074 A1	09-04-2003	SEGAL et al.	

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			Art Unit	2818 2823	
			Examiner Name	TBA M. Estrada	
Sheet	2	of	4	Attorney Docket Number	112020.147US2 NAN-23

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US-2004/0214367 A1	10-28-2004	SEGAL et al.

FOREIGN PATENT DOCUMENTS					
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		Number-Kind Code ² (if known)			
ASE		WO 01/44796 A1	06-21-2001	Board of Trustees of Leland Stanford Junior University	
ASE		WO 01/03208 A1	01-11-2001	President and Fellows of Harvard College	

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
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	A4	WOLF, S., <i>Silicon Processing for the VLSI Era; Volume II – Manufacturing Yield and Reliability Issues of VLSI Interconnects</i> , 1991, Lattice Press, Sunset Beach, pp. 260-273 .		
	A5	WOLF, S., <i>Multilevel-Interconnect Technology for VLSI and ULSI</i> , 1990, Lattice Press, Sunset Beach, pp. 189-191.		
ASE	A6	TOUR, J. M. et al., "NanoCell Electronic Memories," <i>J. Am. Chem Soc.</i> , 2003, Vol. 125, ppl 13279-13283.		

Examiner Signature	<i>M. Estrada</i>	Date Considered	12/12/05
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			Art Unit	2818 2823
			Examiner Name	TBA M. Estrada
			Attorney Docket Number	112020.147US2 NAN-23
Sheet	3	of	4	

hpl	A7	RUECKES, T., et al., "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing" <i>Science</i> , 2000, Vol. 289, pp. 94-97.	
	A8	FAN, S. et al., "Carbon nanotube arrays on silicon substrates and their possible application," <i>Physica E</i> , 2000, Vol. 8, pp. 179-183.	
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	A15	HOMMA, Y. et al., "Growth of Suspended Carbon Nanotubes Networks on 100-nm-scale Silicon Pillars," <i>Appl. Phys. Lett.</i> , 2002, Vol. 81(12), pp. 2261-2263.	
	A16	AJAYAN, P.M., et al., "Nanometre-size tubes of carbon," <i>Rep. Prog. Phys.</i> , 1997, Vol. 60, pp. 1025-1062.	
	A17	SREEKUMAR, T.V., et al., "Single-wall Carbon Nanotube Films", <i>Chem. Mater.</i> 2003, Vol. 15, pp. 175-178.	
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	A19	FUHRER, M.S. et al., "High-Mobility Nanotube Transistor Memory," <i>Nano Letters</i> , 2002, Vol. 2(7), pp. 755-759.	
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	A21	FARAJIAN, A. A. et al., "Electronic transport through bent carbon nanotubes: Nanoelectromechanical sensors and switches," <i>Phys. Rev. B</i> , 2003, Vol. 67, pp. 205423-1 - 205423-6.	
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	A23	LEE, K.H. et al., "Control of growth orientation for carbon nanotubes," <i>Appl. Phys. Lett.</i> , 2003, Vol. 82(3), pp. 448-450.	
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	A25	AMI, S. et al., "Logic gates and memory cells based on single C ₆₀ electromechanical transistors," <i>Nanotechnology</i> , 2001, Vol. 12, pp. 44-52.	
	A26	DEHON, A., "Array-Based Architecture for FET-Based, Nanoscale Electronics," <i>IEEE Transactions on Nanotechnology</i> , 2003, Vol. 2(1), pp. 23-32.	

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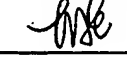
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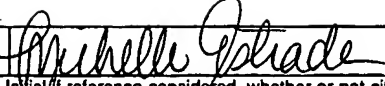
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	A27	TANS, S. et al., "Room-temperature based on a single carbon nanotube," <i>Nature</i> , 1998. Vol. 393, pp. 49-52.	
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